CONFERENCE PROGRAMME

20th EUROPEAN SYMPOSIUM
RELIABILITY OF ELECTRON DEVICES, FAILURE PHYSICS AND ANALYSIS

Bordeaux - France
5 - 9 October 2009

with the technical co-sponsorship of :
IEEE - Electron Devices Society
IEEE – Reliability Society

in conjunction with : **- France and** **- Germany**

organised by : **Laboratoire** **- CNRS**
Université Bordeaux 1 – ENSEIRB

and by :

Monday, October 5, afternoon

13:00 **Registration**

Auditorium

14:00 **Tutorial T1**

"Thermal Management of power electronics systems" *by Eckard WOLFGANG (ECPE, Germany) and Uwe SCHEUERMANN (Semikron, Germany)*

In a power electronics system many sources for thermal losses exist. They are due to on-state and switching losses of active devices, but also passive devices and busbars contribute. When the type of cooling is fixed - either natural convection, forced air cooling or liquid cooling - the thermal pathes from the heat source to the coolant can be designed. The overall goal is to keep thermal resistances as low as possible. In high-voltage systems the insulation is a necessety which has to be inserted in the thermal paths. In addidion to put several components together thermal interface materials are needed. Following the building-in reliability concept the thermal design and it's verification are demonstrated using an IGBT converter. Important data of components and materials are provided as well as concepts for intelligent testing.

15:40 **Coffee break**

16:00 **Workshop : Reliability in harsh environment: application in transportation and industrial environment**

Moderators : Eckard WOLFGANG (ECPE, Germany)
Hélène FREMONT (IMS – University of Bordeaux - France)

18:00 **End of session**

Tuesday, October 6, morning

08:30 **Registration**

Auditorium

08:50 **Tutorial T2**

"MEMS Reliability: Where are we now?"
by Danelle M. TANNER (Sandia National Laboratories, USA)

MicroElectroMechanical Systems (MEMS) technology offers considerable potential due to small size, small weight, and low power of fabricated devices which can enable compelling advantages in certain product specifications. There have been significant successes in MEMS products, most notably ink-jet print heads, accelerometers, and micro-mirror projector systems. However, MEMS reliability is challenging and can be device and process dependent. This tutorial will review the current status of MEMS reliability. The reliability concerns of various devices will be discussed including accelerometers, pressure gauges, RF switches and resonators, and micro-mirror arrays. Additionally, the packaging method and environment will be discussed as part of the whole reliability program. Specifically, the effect of hydrocarbon contamination on metal switches and the subsequent increase in contact resistance over time will be reviewed. MEMS-specific solutions like wafer-level packaging and the effect on reliability will be discussed.

10:30 **Coffee break**

Auditorium

10:50 **Tutorial T3**

"Physical Mechanisms and Modeling of the Bias Temperature Instability"
by Tibor GRASSER (Technische Universität Wien, Institute for Microelectronics, Austria)

Modeling efforts of negative bias temperature instability date back to the work of Jeppson and Svensson in 1977, who proposed the basic form of the popular reaction-diffusion model.
This idea is still at the heart of many modeling attempts today. Recent research indicates, however, that these models cannot capture many crucial aspects of the phenomenon. Consequently, alternative models have been developed which also consider the impact of hole trapping. This tutorial attempts to give a broad review of published modeling attempts, comparing their strengths and weaknesses.

ROOM 2.1/2.4, Second floor

10:50 **Tutorial T4**

"ESD testing of devices, ICs and systems"
by Theo SMEDES (NXP Semiconductors, The Netherlands)

There is a wide range of different ESD stressing methods: (vf-)TLP, HBM, MM, CDM, system level ESD …The key to relate results of different tests to each other is knowledge of the test conditions and device behavior. Therefore this tutorial starts with a brief overview of the different ESD standards, in which the most recent updates will be highlighted. This is followed by a discussion of suitable device characterization techniques. To predict or understand the results of any ESD test, it is essential to know how the devices behave under ESD circumstances (i.e. high currents, short duration). The work horse of ESD device characterization is the well-known Transmission Line Pulse (TLP) technique.
After an overview of the classical TLP implementations, the applications and limitations of this characterization technique will be discussed. For optimum TLP results dedicated test structures need to be available. Test structure design requirements will be explained. It will be illustrated how TLP results relate to classical component level ESD models, such as HBM and MM. It will also be shown why the relation with CDM and system level ESD is much less straightforward. Therefore it will be explored how state-of-the-art TLP extensions can help to close the gaps between the classical ESD device characterization and ESD component/system level performance.
The tutorial will conclude with a discussion on ESD requirements for products.

12:30 **Lunch**

Tuesday, October 6, afternoon

14:00		**Official opening of ESREF 2009** **Chairpersons : N. Labat, D. Lewis (IMS, University of Bordeaux – France)**
14:20	**IP1**	**Opening Conference :** "Process dependence of BTI reliability in advanced HK MG stack" Xavier GARROS *(CEA-LETI – France)*
15:00		**Invited Conference : Best Paper at IRPS 2009** "The Effect of a Threshold Failure Time and Bimodal Behavior on the Electromigration Lifetime of Copper Interconnects" Ronald G. Filippi, Jr.et al. *(IBM – USA)*, presented by Jim LLOYD *(College of Nanoscale Science and Engineering, University of New York – USA)*
15:20		**Invited Conference : Best Paper at IPFA 2009** "Can a MOSFET survive from multiple breakdowns?" X. Li, C.H. Tung, K.L. Pey *(Nanyang Technological University(NTU) and Institute of Microelectronics – Singapore)* presented by N. RAGHAVAN *(NTU – Singapore)*
15:40		**Coffee break**
SESSION A		**Quality and Reliability Techniques for Devices and Systems** **Auditorium**
		Chairs : V. Loll (Nokia – Denmark) F. Fantini (University of Modena – Italy)
16:00	**A1**	Electrical aging behavioural modelling for reliability analyses of ionizing dose effects on an n-MOS simple current mirror C. Bestory[a], F. Marc[a], S. Duzellier[b] b, H. Levi[a] ([a]*IMS Lab. – University of Bordeaux,* [b]*ONERA Centre de Toulouse – France)*
16:20	**A2**	Correlation between EOS customer return failure cases and Over Voltage Stress (OVS) test method J.-L. Lefebvre, C. Gautier, F. Barbier *(NXP Semiconductors, LaMIPS Univ. Caen – France)*
16:40	**A3**	Fast Reliability Qualification of SiP products C. Regard[1, 2, 3], C. Gautier[1, 2], H. Frémont[3], P. Poirier[1, 2], X. Ma[4], K. M.B. Jansen[4] *([1]NXP Semiconductors, [2]LaMIPS Univ. Caen, [3]IMS Lab. Univ. Bordeaux – France, [4]Delft University of Technology, the Netherlands)*
17:00	**A4**	Electromagnetic immunity model of an ADC for microcontroller's reliability improvement J.-B. Gros[1], G. Duchamp[1], A. Meresse[†], J.-L. Levant[2] ([1] *IMS Lab. Univ. Bordeaux,* [2]ATMEL NANTES – France)
17:20	**A5**	Comparison and evaluation of newest failure rate prediction models: FIDES and RIAC 217Plus M. Held[1], Klaus Fritz[2] *([1]Swiss Federal Institute for Materials Testing and Research, EMPA - Switzerland, [2]Diehl Aerospace GmbH - Germany)*
17:40		**Presentation of their activity by exhibitors**
17:40 to 18:00		**Author's corner for session A**

Wednesday, October 7, morning

Session F		**Extreme environments: Power devices reliability** **Auditorium**
		Chairs: E. Wolfgang (Siemens - Germany) M. Ciappa (ETH Zürich - Switzerland)
8:30	**IP2**	**Invited Conference :** "Reliability challenges of automotive power electronics" by Uwe SCHEUERMANN *(Semikron Elektronik GmbH & Co. KG – Germany)*
9:10	**F1**	Characterization of ageing failures on Power MOSFET Devices by electron and ion microscopies D. Martineau[a], T. Mazeaud[b], M. Legros[a], Ph. Dupuy[b], C. Levadea[c], G.Vanderschaevea[c] *([a]CEMES-CNRS, [b]Freescale Semiconductors,* [c]Université de Toulouse, INSA – France)
9:30	**F2**	A New Built-In Screening Methodology to Achieve Zero Defects in the Automotive Environment V. Malandruccolo[1], M. Ciappa[1], H. Rothleitner[2], W. Fichtner *([1]Swiss Federal Institute of Technology (ETH) – Integrated Systems Laboratory - Switzerland, [2]Infineon Technologies AG – Austria)*
9:50	**F3**	Source electrode evolution of a low voltage power MOSFET under avalanche cycling B.Bernoux[1,2,3], R.Escoffier[3], P.Jalbaud[3], J.M.Dorkel[1,2] *([1]CNRS; LAAS; [2]Université de Toulouse; UPS, INSA, INP, ISAE; LAAS; [3]Freescale Semiconducteurs France SAS – France)*
10:10	**F4**	Thermal imaging of smart power DMOS transistors in the thermally unstable regime using a compact transient interferometric mapping system G. Haberfehlner[a], S. Bychikhin[a], V. Dubec[a], M. Heer[a], A. Podgaynaya[b], M. Pfost[b], M. Stecher[b], E. Gornik[a], D. Pogany[a] *([a]Institute for Solid State Electronics, Vienna University of Technology – Austria, [b]Infineon Technologies – Germany)*
10:30		**Coffee break**
Session F cont'd		**Extreme environments: Power devices, Aeronautic and Spatial electronics reliability** **Auditorium**
		Chairs: E. Wolfgang (Siemens - Germany) M. Ciappa (ETH Zürich - Switzerland)
10:50	**F5**	Reliability considerations in pulsed power resonant conversion F. Carastro, A. Castellazzi, J. Clare, M. Johnson, M. Bland, P. Wheeler *(University of Nottingham, Department of Electrical and Electronic Engineering - UK)*
11:10	**F6**	Estimation of SiC JFET temperature during short-circuit operations M. Berkani[1], S. Lefebvre[1], N. Boughrara[1,2], Z. Khatir[3], J.-C. Faugières[1], P. Friedrichs[4], A. Haddouche[5] *([1]SATIE CNAM, ENS Cachan, CNRS, UniverSud – France, [2]Skikda university, Département d'électromécanique – Algérie, [3]LTN INRETS – France, [4]SICED – Germany, [5]Faculté des Sciences de l'ingénieur Université Badji Mokhtar Annaba – Algérie)*
11:30	**F7**	Instable Mechanisms During Unclamped Operation of High Power IGBT Modules G. Busatto, C. Abbate, F. Iannuzzo, P. Cristofaro *(Dept. of Automation, Electromagnetism, Information Engineering and Industrial Mathematics, University of Cassino – Italy)*

11:50	**F8**	An Investigation into the Reliability of Power Modules considering Base Plate solders Thermal Fatigue in Aeronautical Applications A. Micol[a], A. Zeanha[b,d], T. Lhommeau[c], S. Azzopardi[d], E. Woirgard[d] *([a]Université de Toulouse, ENIT/LGP, [b]PEARL, [c]Hispano-Suiza, [d]IMS, Université de Bordeaux – France)*
12:10	**F9**	Accelerated Active Ageing Test on SiC JFETs Power Module with Silver Joining Technology for High Temperature Application L. Dupont[a], G. Coquery[a], K. Kriegel[b], A. Melkonyan[b] *([a]LTN INRETS, INRETS – France, [b]SIEMENS Corporate Technology – Germany)*
12:30	**12:50**	**Author's corner for session F, First floor**

SESSION C1	**Electron and Optical Beam Test** **Room 2.1/2.4, Second floor**

Chairs: R. Heiderhoff (University of Wuppertal - Germany)
V. Pouget (IMS, University of Bordeaux – France)

10:50	**IP3**	**Invited Conference :** "Laser THz emission microscope as a novel tool for LSI failure analysis" Masatsugu YAMASHITA *(RIKEN – Japan)*
11:30	**C1**	Jitter Analysis of PLL-Generated Clock Propagation using Jitter Mitigation Techniques with Laser Voltage Probing J.Y. Liao[a], T. Ton[a], N. Slattengren[a], S. Kasapi[a], W. K. Lo[a], H. L. Marks[a], Yin S. Ng[b], T. Lundquist[b] *([a]NVIDIA Corporation, [b]DCG System Inc. - USA)*
11:50	**C2**	IR thermography and FEM simulation analysis of on-chip temperature during thermal-cycling power-metal reliability testing using in-situ heated structures H. Köck[a,b], V. Košela[c], C. Djelassi[a], M. Glavanovics[a], D. Pogany[b] *([a]KAI GmbH, [b]Institute for Solid State Electronics, Vienna University of Technology - Austria, [c]Slovak University of Technology in Bratislava – Slovakia)*
12:10	**C3**	Investigation on marginal failure characteristics and related defects analysed by Soft Defect Localization C. Hartmann , M. Wieberneit (*NEC Electronics Europe* – Germany)
12:30	**12:50**	**Author's corner for session C1, First floor**

12:50		**Lunch**

Wednesday, October 7, afternoon

SESSION E		**Packaging, passive components and MEMS** **Auditorium**
		Chairs: H. Frémont, (IMS-University of Bordeaux - France) W. Wondrak, (DaimlerChrysler – Germany)
14:00	**IP4**	**Invited Conference :** "Quasi hermetic packaging for new generation of space-borne microwave equipment" Philippe MONFRAIX *(Thales Alenia Space – France)*
14:40	**E1**	A new methodology for the identification of ball bond degradation during high-temperature aging tests on devices in standard plastic packages M.A. Bahi[a], H. Frémont[b], J.P. Landesman[c], A. Gentil[a], P. Lecuyer[a] *([a]ATMEL Nantes SA, [b]IMS University of Bordeaux, [c]IMN, NANTES – France)*
15:00	**E2**	Multiscale Simulation of Aluminum Thin Films for the Design of Highly-Reliable MEMS Devices H. Kubo[1], M. Ciappa[2], T. Masunaga[1], and W. Fichtner[2] *([1]Toshiba Corp. – Japan, [2]Swiss Federal Institute of Technology (ETH) – Switzerland)*
15:20	**E3**	A novel accelerated test technique for assessment of mechanical reliability of solder interconnects G. Khatibi[1], W. Wroczewski[1], B. Weiss[1], H. Ipser[2] *([1]University of Vienna, Faculty of Physics, [2]University of Vienna, Department of Inorganic Chemistry/Materials Chemistry – Austria)*
15:40		**Author's corner for session E, First floor**
16:00		**Coffee break**
SESSION C1/C2		**Advanced Techniques for Failure Analysis and case studies** **Room 2.1/2.4, Second floor**
		Chairs: Ph. Perdu (CNES - France) M. Vanzi (University of Cagliari – Italy)
14:00	**IP5**	**Invited Conference :** "Physical Analysis, Trimming and Editing of Nanoscale IC Function with Backside FIB Processing" Rudolf SCHLANGEN *(Berlin University of Technology – Germany)*
14:40	**C4**	Electrical modeling of the effect of beam profile for pulsed laser fault injection C. Godlewski[1], V. Pouget[2], D. Lewis[2], M. Lisart[1] *([1]STMicroelectronics, [2]IMS, University of Bordeaux – France)*
15:00	**C5**	Finite Element Analyses assisted Scanning Joule Expansion Microscopy on Interconnects for Failure Analysis and Reliability Investigations A.-K. Tiedemann[a], K. Kurz[a,b], M. Fakhri[a,b], R. Heiderhoff[a], J.C.H. Phang[b], and L.J. Balk[a,b] *([a]Faculty of Electrical, Information and Media Engineering, University of Wuppertal – Germany, [b]Centre for Integrated Circuit Failure Analysis and Reliability (CICFAR), National University of Singapore – Singapore)*

15:20	**C6**	Magnetic Microscopy for 3D devices: defect localization with high resolution and long working distance on complex System in Package F.Infante[a], P.Perdu[a], D.Lewis[b] *([a]CNES, [b]IMS, University of Bordeaux – France)*
15:40	**C7**	Net integrity checking by optical localization techniques G. Haller[a] , A. Machouat[a], D. Lewis[b] , V. Pouget[b] *([a]STMicroelectronics Rousset, [b]IMS, University of Bordeaux – France)*

16:00 Author's corner for sessions C1 & C2, First floor

16:20 Coffee break

16:40 to 18:00 Poster Session (first floor, salle des Ambassadeurs)

18:00 to 19:30 Workshop (Auditorium)

EUFANET : European Failure Analysis Network

Moderators : Philippe Perdu (CNES - France)
Felix Beaudoin (IBM - USA)

Tentative schedule:

18:00: Welcome & EUFANET status (Philippe Perdu, CNES)
18:10: Introduction to 3D packages FA challenges (Pete Jacob, EMPA)
18:30: High Resolution, 3D short circuits localization by magnetic microscopy (Fulvio Infante, CNES)
18:45: Open detection by SQUID (Infineon)
19:00: Chip access (Digitconcept)
19:20: Wrap-up

Thursday, October 8
Auditorium

SESSION B2 — **Failure Mechanisms in Si technologies and Nanoelectronics (Low K materials, Cu interconnects, ESD ...)**

Chairs:
M. Bafleur (LAAS CNRS Toulouse – France)
H. Gieser (Fraunhofer IZM München - Germany)

08:30 **IP6** **Invited Conference**

"Do ESD fails in systems correlate with IC ESD robustness?"
Wolfgang STADLER *(Infineon Technologies – Germany)*

09:10 **B2-1** Electromigration in width transition copper interconnect

A. Roy[a], Y. Hou[b], C. M. Tan[b]
([a]Department of Electronics, West Bengal State University – India, [b]School of Electrical and Electronic Engineering, Nanyang Technological University – Singapore)

09:30 **B2-2** Investigation of Stress Distribution in Via Bottom of Cu-Via Structures with different Via form by means of Submodeling

J. Ciptokusumo, K. Weide-Zaage, Oliver Aubel* (Laboratorium für Informationstechnologie, Leibniz Universität Hannover, *GLOBALFOUNDRIES Inc – Germany)

09:50 **B2-3** A Methodology to Extract Failure Rates for Low-K Dielectric Breakdown with Multiple Geometries and in the Presence of Die-to-Die Linewidth Variation

M. Bashir, L. Milor *(School of Electrical and Computer Engineering, Georgia Institute of Technology – USA)*

10:10 **B2-4** Failure Mechanisms of Discrete Protection Device subjected to Repetitive ElectroStatic Discharges (ESD)

M. Diatta[a,b,c], E. Bouyssou[a], D. Trémouilles[b,c], P. Martinez[a], F. Roqueta[a], O. Ory[a], M. Bafleur[b,c] *([a]STMicroelectronics, [b]CNRS, LAAS, [c]Université de Toulouse, UPS, INSA, INP, ISAE, LAAS – France)*

10:30 **Author's corner for sessions B2, First floor**

10:50 **Coffee break**

SESSION E — **Packaging, passive components and MEMS**
Auditorium

Chairs: H. Frémont (IMS-University of Bordeaux - France)
W. Wondrak (DaimlerChrysler – Germany)

11:10 **IP7** **Invited Conference**

"Design for reliability of power electronics modules"

Chris BAILEY et al. *(Computational Mechanics and Reliability Group, University of Greenwich – United Kingdom)*

11:50 **E4** Accelerated lifetime test of RF-MEMS switches under ESD stress

J. Ruan[a,b], N. Nolhier[a,b], G. J. Papaioannou[a,c], D. Trémouilles[a], V. Puyal[a], C. Villeneuve[a], T. Idda[a], F. Coccetti[a] , R. Plana[a,b] *([a]LAAS-CNRS, [b]University of Toulouse - France [c]University of Athens, Physics Dpt. – Greece)*

12:10 **E5** Characterisation of power modules ceramic substrates for reliability aspects

S. Pietranico[a,b], S. Pommier[a], S. Lefebvre[b], Z. Khatir[c], S. Bontemps[d]
([a]LMT-Cachan, ENS Cachan, CNRS, UPMC, UniverSud Paris, [b]SATIE, ENS Cachan, CNRS, CNAM, UCP, UniverSud Paris, [c]INRETS-LTN, [d] Microsemi PPG – France)

12:30 **E6** Microstructure evolution observation for SAC solder joint. Comparison between thermal cycling and thermal storage

M.Berthou[1,2,3], P.Retailleau[1], H.Frémont[2], A.Guédon-Gracia[2], C.Jéphos-Davennel[3]
([1]MBDA France, [2]IMS, University of Bordeaux, [3]DGA CELAR – France)

12:50 **Author's corner for session E, First floor**

13:10 **Lunch**

SESSION B1 **Failure Mechanisms in Si technologies and Nanoelectronics : NBTI**
Auditorium

Chairs : C. Salm (University of Twente – The Netherlands)
N. Stojadinovic (University of Niš - Serbia)

14:20 **Invited Conference: Best Paper of the 2009 Japan Reliability Conference (RCJ)**

"Study for Pulse Stress NBTI Characteristics Degradation"

Nozomu KAWAI, Yasuhiro Dohi, Nobuyuki Wakai *(Toshiba Corporation Semiconductor Company – Japan)*

14:40 **B1-1** NBTI and hot-carrier effects in accumulation-mode Pi-gate pMOSFETs

C.-W. Lee[a], I. Ferain[a], A. Afzalian[a], R. Yan[a], N. Dehdashti[a], P. Razavi[a], J.-P. Colinge[a] and J. T. Park[b] *([a]Tyndall National Institute – Ireland, [b]Department of Electronics Engineering, University of Incheon – Korea)*

15:00 **B1-2** Impact of O-Si-O bond angle fluctuations on the Si-O bond-breakage rate

S. Tyaginov[1], V. Sverdlov[2], I. Starkov[1], W. Gös[1], T. Grasser[1]
([1]Christian Doppler Laboratory for TCAD at the Institute for Microelectronics, [2]Technische Universität Wien, - Austria)

15:20 **B1-3** Effects of low gate bias annealing in NBT stressed p-channel power VDMOSFETs

I. Manić[a], D. Danković[a], S. Djorić-Veljković[b], V. Davidović[a], S. Golubović[a], and N. Stojadinović[a] *([a]Faculty of Electronic Engineering, University of Niš, [b]Faculty of Civil Engineering and Architecture, University of Niš – Serbia)*

15:40 **B1-4** Influence of various process steps on the reliability of PMOSFETs submitted to Negative Bias Temperature Instabilities

C. Bénard[1,3], G. Math[1,3], P. Fornara[1], J.-L. Ogier[1], D. Goguenheim[2,3]
([1]ST Microelectronics, Rousset, [2]ISEN-Toulon, IM2NP, [3]IM2NP-Toulon, France)

16:00 **B1-5** On the Temperature and Voltage Dependence of Short-Term Negative Bias Temperature Stress

Ph. Hehenberger[1], P.-J. Wagner[2], H. Reisinger[3] and T. Grasser[2]
([1]Institute for Microelectronics, TU Wien, [2]Christian Doppler Laboratory for TCAD at the Institute for Microelectronics, TU Wien – Austria, [3]Infineon Technologies – Germany)

16:20 **Coffee break**

SESSION B1		Failure Mechanisms in Si technologies and Nanoelectronics: Oxide reliability Auditorium
		Chairs : C. Salm (University of Twente – The Netherlands) N. Stojadinovic (University of Niš - Serbia)
16:40	**B1-6**	Investigation of defects introduced by static and dynamic hot carrier stress on SOI partially depleted body-contact MOSFETs M.A.Exarchos[1], G.J.Papaioannou[1], J.Jomaah[2], F.Balestra[2] *([1]Physics Department, National and Kapodistrian, University of Athens – Greece, [2]IME Grenoble INP-Minatec – France)*
17:00	**B1-7**	Reversible Dielectric Breakdown in ultrathin Hf based high-k stacks under current limited stresses A. Crespo-Yepes, J. Martin-Martinez, R. Rodriguez, M. Nafria and X. Aymerich *(Dept. Electrical Engineering, Universitat Autònoma de Barcelona (UAB) – Spain)*
17:20	**B1-8**	Effects of electromagnetic near field stress on SiGe HBT's reliability A. Alaeddine[a,b], M. Kadi[b], K. Daoud[a], B. Mazari[b] *([a] GPM, University of Rouen, [b]IRSEEM / ESIGELEC – France)*
17:40	**B1-9**	Experimental Study about Gate Oxide Damages in Patterned MOS Capacitor Irradiated with Heavy Ions G. Busatto[a], G. Currò[b], F. Iannuzzo[a], A. Porzio[a], A. Sanseverino[a], F. Velardi[a] *([a]Dept. of Automation, Electromagnetism, Information Engineering and Industrial Mathematics, University of Cassino, [b]ST-Microelectronics – Italy)*

18:00 to 18:20	Author's corner for session B1, First floor

Friday, October 9, morning

SESSION D		**Failure Mechanisms in Microwave and High Band-Gap** **Auditorium**
		Chairs: G. Meneghesso (University of Padova - Italy) J. Wüffl (FBH Berlin - Germany)
08:30	**IP8**	**Invited Conference** "GaN HEMT Reliability" Jesus A. del ALAMO, J. Joh *(Massachusetts Institute of Technology – USA)*
09:10	**D1**	Reliability analysis of AlGaN/GaN HEMT on SopSiC composite substrate under long term DC life test N. Ronchi, F. Zanon, A. Stocco, A. Tazzoli, E. Zanoni and G. Meneghesso *(Dept. of Information Engineering, University of Padova – Italy)*
09:30	**D2**	Characterization of stress degradation effects and thermal properties of AlGaN/GaN HEMTs with photon emission spectral signatures A. Glowacki[1], P. Laskowski[1], C. Boit[1], P. Ivo[2], E. Bahat-Treidel[2], R. Pazirandeh[2], R. Lossy[2], J. Würfl[2], G. Tränkle[2] (*[1]Department of Semiconductor Devices, Berlin University of Technology, [2]Ferdinand Braun Institut für Höchstfrequenztechnik, Berlin – Germany)*
09:50	**D3**	Characterisation and modelling of parasitic effects and failure mechanisms in AlGaN/GaN HEMTs N. Malbert[1], N.Labat[1], A. Curutchet[1], C. Sury[1], V. Hoel[2], J.-C. de Jaeger[2], N. Defrance[2], Y. Douvry[2], C. Dua[3], M. Oualli[3], C. Bru-Chevallier[4], J.-M. Bluet[4], W. Chikhaoui[4] *([1]IMS, University of Bordeaux, [2]IEMN, Université Lille 1, [3]ALCATEL –THALES -3-5 Lab, [4]INL, INSA Lyon – France)*
10:10		**Author's corner for session D, First floor**
10:30		**Coffee break**
SESSION D		**Failure Mechanisms in Photonic Devices**
		Chairs: G. Meneghesso (University of Padova - Italy) J. Wüffl (FBH Berlin - Germany)
10:50	**IP9**	**Invited Conference** "Towards Reliable Thin-Film Encapsulation of Organic Electronic Devices" Thomas RIEDL *(TU Braunschweig – Germany)*
11:30	D4	Analysis of humidity effects on the degradation of high-power white LEDs C. M. Tan[1, 2], B. K. E. Chen[2], G. Xu[3], Y. Liu[3] *([1]School of Electrical and Electronic Engineering, Nanyang Technological University, [2]Singapore Institute of Manufacturing Technology, [3]National Metrology Centre - Singapore)*
11:50	D5	Life-time estimation of High-power Blue Light-Emitting Diode Chips Jeung-Mo Kang, Jeong-Hyeon Choi, Du-Hyun Kim, Jae-Wook Kim and Ho-Ki Kwon *(LED R &D Center, LED Division, LG Innotek - Republic of Korea)*
12:10	D6	Reliability analysis of InGaN Blu-Ray Laser Diode N. Trivellin[1], M. Meneghini[1], G. Meneghesso[1], E. Zanoni[1], K. Orita[2], M. Yuri[2], T. Tanaka[2], D. Ueda[2] *([1]University of Padova, Department of Information Engineering - Italy, [2]Panasonic Corporation – Japan)*

9:00 to 12:30	**2nd LOTUS Workshop** **Room 2.1/2.4, Second floor**

Tentative schedule:

9:10: Welcome (Philippe Perdu CNES)
9:15: LOTUS introduction: 1st workshop results and follow up (Laurent Cretinon, EDF)
9:25: Commercial parts: what can end user do (Part 1)
- 9:25 Evaluation test program for Deep Submicron monolithic integrated circuits (Horst Geiser, Fraunhofer IZM)
- 10:05 Risk analysis (Florian Moliere, EADS IW)

10:30 Coffee break
10:50: Commercial parts: what can end user do (Part 2)
- 10:50 Margin Analysis (Amjad Deyine, Thales ISS)
- 11:15 Reliability Improvement in Electronic Devices (Michael Hertl, INSIDIX)

11:40: Status of reliability activities (Laurent Cretinon, EDF)
12:00: Round table: white book, reliability specification and other end users needs (moderator to be defined)
s12:25: conclusion

12:30	**Announcement of ESREF 2009 Best Paper Awards** **ESREF 2010 Announcement** **Conference closing**

POSTERS

The Poster session is scheduled on Wednesday, October 7 from 16:40 to 18:00.

SESSION A Quality and Reliability Techniques for Devices and Systems

AP1 Ensuring the reliability of electron beam crosslinked electric cables by the optimization of the dose depth distribution with Monte Carlo simulation

M. Ciappa[a], L. Mangiacapra[a], M. Stangoni[b], S. Ott[b], W. Fichtner[a]
([a]Swiss Federal Institute of Technology (ETH), Integrated Systems Laboratory, ETH-Zentrum, [b]HUBER+SUHNER AG, Wire+Cable Division, R&D – Switzerland)

AP2 CMOS Logic Gate Performance Variability Related to Transistor Network Arrangements

D. N. da Silva, A. I. Reis, R. P. Ribas *(PGMicro - Federal University of Rio Grande do Sul – Brazil)*

SESSION B1 Characterisation and Modelling of Failure Mechanisms in Silicon technologies and Nanoelectronics (Hot carriers, NBTI, High K gate materials, ...)

BP1 Behavior of Hot Carrier Generation in Power SOI LDNMOS with Shallow Trench Isolation (STI)

J. Liao[1, 2], C. M. Tan[1] and G. Spierings[2]
([1]School of Electrical and Electronic Engineering, Nanyang Technological University, [2]Systems on Silicon Manufacturing Co Pte Ltd – Singapore)

BP2 NBTI and hot carrier effect of SOI p-MOSFETs fabricated in strained Si SOI wafer

Y. Jeon[a], D. H. Ka[a], C. G. Yu[a], W.-J. Cho[b], M. Saif Islam[c], and J. T. Park[a]
([a]Department of Electronics Engineering, University of Incheon, [b]Department of Electronic Materials Engineering, Kwangwoon University – Korea, [c]Department of Electrical and Computer Engineering, University of California – USA)

BP3 Modelling and experimental verification of the impact of negative bias temperature instability on CMOS inverter

N. Berbel, R. Fernandez, I.Gil
(Dept. d'Enginyeria Electrònica, Universitat Politècnica de Catalunya, - SPAIN)

BP4 Effects of the electrical stress on the conduction characteristics of metal gate/MgO/InP stacks

E. Miranda[1], J. Martin-Martinez[1], E. O'Connor[2], G. Hughes[3], P. Casey[3], K. Cherkaoui[2], S. Monaghan[2], R. Long[2], D. O'Connell[2] and P.K. Hurley[2] *([1]Escola Tècnica Superior d'Enginyeria, Universitat Autònoma de Barcelona - Spain, [2]Tyndall National Institute, University College Cork, [3]School of Physical Sciences, Dublin City University, - Ireland)*

BP5 Extraction of 3D parasitic capacitances in 90nm and 22nm NAND Flash Memories

J. Postel-Pellerin[1], F. Lalande[1], P. Canet[1], R. Bouchakour[1], F. Jeuland[2], B. Bertello[2], B. Villard[2]
([1]Aix-Marseille Université, IM2NP, [2]ATMEL Corporation, Device Engineering – France)

BP6 Modeling charge variation during data retention of MLC Flash Memories

J. Postel-Pellerin[1], F. Lalande[1], P. Canet[1], R. Bouchakour[1], F. Jeuland[2], L. Morancho[2]
([1]Aix-Marseille Université, IM2NP, [2]ATMEL Corporation, Device Engineering – France)

BP7 Statistical RTS model for digital circuits

L. Brusamarello, G. I. Wirth, R. da Silva (*Universidade Federal do Rio Grande do Sul – Brazil)*

BP8 A Modelisation of the Temperature dependence of the Fowler-Nordheim current in EEPROM Memories

M. Roca[1], R. Laffont[1], G. Micolau[1], F. Lalande[1], O. Pizzuto[2]
([1]Aix-Marseille Université, IM2NP, [2]ST-Microelectronics – France)

BP9 Percolation Theory Applied to PZT Thin Films Capacitors Breakdown Mechanisms

M.T. Chentir[1,2], J.-B. Jullien[2], B. Valtchanov[2], E. Bouyssou[2], L. Ventura[1], C. Anceau[2]
([1]François Rabelais University, Laboratoire de Microélectronique de Puissance, [2]STMicroelectronics – France)

SESSION B2 — Characterisation and Modelling of Failure Mechanisms in Silicon technologies and Nanoelectronics (Low K materials, Cu interconnects, ESD, ...)

BP11 Impacts and damages on deep sub-micronic CMOS technology induced by substrate current due to ESD stress

Ph. Galy, S. Dudit, M. Vallet, C. Richier, C. Entringer, F Jezequel, E. Petit, J. Beltritti *(STMicroelectronics – France)*

BP12 Breakdown Characterization of Gate Oxides in 35 and 70 Å BCD8 Smart Power Technology

A. Tazzoli[a], L. Cerati[b], A. Andreini[b], G. Meneghesso[a]
([a]University of Padova, Department of Information Engineering, [b]STMicroelectronics TR&D - Smart Power & High Voltage Tech. Plat. Dev. - Italy

SESSION C — Advanced Techniques for failure analysis and Case studies: Electron and Optical Beam Testing (EOBT) and new characterisation techniques

CP1 An Advanced Quality and Reliability Assessment Approach Applied to Thermal Stress Issues in Electronic Components and Assemblies

M. Hertl, D. Weidmann, J.-C. Lecomte *(INSIDIX – France)*

CP2 Failure Analysis of Video processor defined as No Fault Found (NFF): Reproduction in system level and Advanced Analysis technique in IC Level

J.-S. Jeong, S.-D. Park
(Advanced Technology Group, CS Management Center, Samsung Electronics CO., LTD – Korea)

CP3 A Study of Electrical Characteristic Changes in MOSFET by Electron Beam Irradiation

Y. Mitsui[a], T. Sunaoshi[a], J. C. Lee[b]
([a]Hitachi High-Technologies Corp. – Japan, [b]Taiwan Semiconductor Manufacturing Company, Ltd. – Taiwan R.O.C.)

CP4 Trapped charge and stress induced leakage current (SILC) in tunnel SiO_2 layers of deprocessed MOS non-volatile memory devices observed at the nanoscale

M.Lanza[1], M.Porti[1], M.Nafría[1], X. Aymerich[1], G. Ghidini[2], A. Sebastiani[2]
([1]Dept. Eng. Electrònica, Universitat Autònoma de Barcelona – Spain, [2]Numonyx – Italy)

CP5 Displacement Current Sensor for Contact and Intermittent Contact Scanning Capacitance Microscopy

R. Biberger[a], G. Benstetter[a], H. Goebel[b]
([a]University of Applied Sciences Deggendorf, [b]Helmut-Schmidt-University – Germany)

CP6 Lot reliability issues in Commercial Off The Shelf (COTS) microelectronic devices

G. Mura[1], M. Vanzi[2]
([1]Telemicroscopy Laboratory Sardegna Ricerche, [2] DIEE-INFM, University of Cagliari – Italy)

SESSION D — Failure Mechanisms in Microwave, High Bandgap and Photonic Devices

DP1 Degradation of TiAlNiAu as ohmic contact metal for GaN HEMTs

M. Piazza[a,b], Ch. Dua[a], M. Oualli[a], E. Morvan[a], D. Carisetti[c],F. Wyczisk[c]
([a]A-T 3-5Lab, [b]XLIM, Faculté des Sciences, [c]THALES RESEARCH & TECHNOLOGY – France)

DP2 Evaluation of AlGaInP LEDs reliability based on accelerated tests.

E. Nogueira Díaz[a], M. Vázquez López[b], N. Núñez Mendoza[b]
([a]Telefónica I+D, EUITT- Universidad Politécnica Madrid, [b]EUITT-Instituto de Energía Solar - Universidad Politécnica Madrid – Spain)

DP3 Fabrication Process Simulation and Reliability Improvement of Highbrightness LEDs

T.-L. Chou, C.-F. Huang, C.-N. Han, S.-Y. Yang, and K.-N. Chiang
(Advanced Microsystem Packaging and Nano-Mechanics Research Lab., Department of Power Mechanical Engineering, National Tsing Hua University - Taiwan R.O.C.)

SESSION E — Packaging, Assemblies, Passive Components and MEMS

EP1 Reading Distance Degradation Mechanisms of Near Field RFID Devices

P. Jacob[a,b], W. Knecht[a], A. Kunz[a], G. Nicoletti[a], T. Lautenschlager[c], M. Mondada[d], D. Pachoud[d]
([a]EMPA Swiss Federal Labs for Materials Testing & Research, [b]EM Microelectronic Marin SA – Switzerland, [c]Sokymat Automotive - Germany, [d]Datamars SA – Switzerland)

EP2 Heat management for power converters in sealed enclosures: a numerical study

M. Bernardoni, P. Cova, N. Delmonte, R. Menozzi
(Universit`a degli Studi di Parma, Dipartimento di Ingegneria dell'Informazione - Italy)

EP3 Comparing Drop Impact Test Method Using Strain Gauge Measurement

Y. Liu[2], F.J.H.G Kessels[1], W.D. van Driel[1,3], J.A.S. van Driel[3], F.L. Sun[2], G.Q. Zhang[1,3]
([1]NXP Semiconductors - The Netherlands, [2]School of Material Science and Engineering, Harbin University of Science & Technology – China, [3]Delft University of Technology - The Netherlands)

EP4 Capacitive RF MEMS analytical predictive reliability

M. Matmat, F. Cocetti, A. Marty, R. Plana, C. Escriba, J.-Y. Fourniols, D. Esteve
(LAAS-CNRS ; Université de Toulouse - France)

EP5 Dielectric Charging in Silicon Nitride Films for MEMS Capacitive Switches: Effect of Film Thickness and Deposition Conditions

U. Zaghloul[a], G. Papaioannou[b], F. Coccetti[a], P.Pons[a] and R. Plana[a]
([a]CNRS-LAAS, [b]Université de Toulouse ; UPS, INSA, INP, ISAE ; LAAS – France, [c]Solid State Physics Section, University of Athens – Greece)

EP6 Numerical prediction of failure paths at a roughened metal/polymer interface

S.P.M. Noijen[a], O. van der Sluis[a,b], P.H.M. Timmermans[a], G.Q. Zhang[b]
([a]Philips Applied Technologies, [b]Department of Precision and Microsystem Engineering, Delft University of Technology - The Netherlands)

SESSION F — Extreme environments : Power devices, aeronautic and spatial electronics reliability

FP1 Analysis of Deep Sub Micron VLSI Technological risks: A new qualification process for professional electronics

F. Molière[a,c], B. Foucher[a], P. Perdu[b], A. Bravaix[c]
([a]EADS France Innovation Work, [b]CNES, [c]ISEN-IM2NP, CNRS - France)

FP2 1300 V, 2 ms pulse inductive load switching test circuit with 20 ns selectable crowbar intervention

L. Rossi, M. Riccio, E. Napoli, A. Irace, G. Breglio, P. Spirito
(Università degli Studi di Napoli "Federico II" Dipartimento di Ingegneria Biomedica Elettronica e delle Telecomunicazioni – Italy)

FP3 Analysis of the dynamic behavior changes of supercapacitors during calendar life test under several voltages and temperatures conditions

H. El Brouji, O. Briat, J-M. Vinassa, H. Henry, E. Woirgard
(Laboratoire IMS, ENSEIRB, Université Bordeaux 1 – France)

FP4 Uni-axial mechanical stress effect on Trench Punch Through IGBT undershort-circuit operation

Y. Belmehdi, S. Azzopardi, A. Benmansour, J.-Y. Delétage, E. Woirgard
(Laboratoire IMS, ENSEIRB, Université Bordeaux 1 – France)